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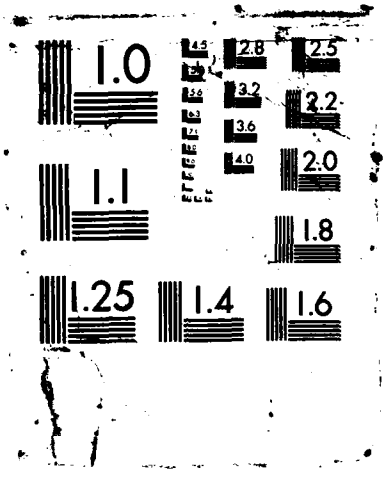
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A planar IC-compatible transferred electron device for millimeter-wave operation

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Contract No. DAJA 45-86-C-0039

"4th Periodic Report"

September 1, 1987 - February 29, 1988

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REPORT DOCUMENTATION PAGE

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1 REPORT NUMBER: 4th report	2 GOVT ACCESSION NO. / 3 RECIPIENT'S CATALOG NUMBER
4 TITLE (and Subtitle): A planar IC - compatible transferred electron device for millimeter-wave operation	5 TYPE OF REPORT & PERIOD COVERED: interim, Sept.87-Feb.88 / 6 PERFORMING ORG. REPORT NUMBER
7 AUTHOR(s): Hartwig W. Thim	8 CONTRACT OR GRANT NUMBER(s): DAJA 45-86-C-0039
9 PERFORMING ORGANIZATION NAME AND ADDRESS: Microelectronics Institute, University of Linz, Altenbergerstr.69, A-4040 Linz,Austria	10 PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11 CONTROLLING OFFICE NAME AND ADDRESS: Contracting Office (Mr.G.B.Evans), 447th Area Support Group, P.O.Box 160, Warrington,Cheshire,England	12 REPORT DATE: March 23, 1988 / 13 NUMBER OF PAGES: seven (7)
14 MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): USARDS Group UK, 223 Old Marylebone Road, London NW1 5TH	15 SECURITY CLASS (of this report) / 15a DECLASSIFICATION DOWNGRADING SCHEDULE

16 DISTRIBUTION STATEMENT (of this Report)

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17 DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18 SUPPLEMENTARY NOTES

19 KEY WORDS (Continue on reverse side if necessary and identify by block number)

Experimental results obtained with E-beam fabricated 0.5µm gate devices; small signal impedance of the device; amplification at 26 - 37 GHz; identification of the circuit elements determining the frequency of operation; 12db/octave fall-off of efficiency.

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

Devices with 0.5µm long gates have been fabricated using E-beam lithography. Since no improvement in efficiency has been obtained it is recommended to use 1-1.5µm long gates which are easy to fabricate. It was also found that finger gate devices exhibit ten times smaller efficiencies (0.1%) than overlapping gate devices do.

In order to produce gain at a desired frequency ($\lambda/2+\epsilon$)-lines terminated by radial stubs must be connected to both gate and source.

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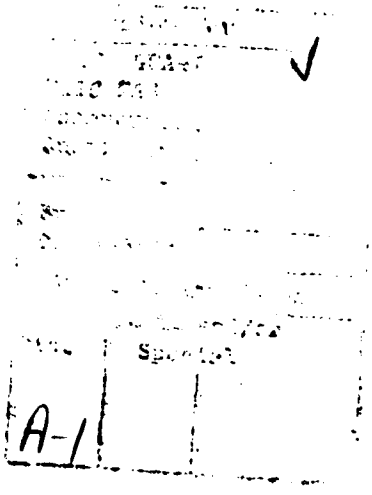
20 Abstract continued

Maximum gain occurs at that frequency at which the capacitive reactances of the lines with $0<\delta<\lambda/4$ compensate for lead and other parasitic inductances.

The device breaks into oscillations when a dielectric resonator with its resonance frequency near the maximum gain frequency is placed near both drain and gate bonding pads. The oscillator frequency can be tuned over a few hundred megahertz by varying the gate voltage by approximately 10%.

An unexpectedly steep (12db/octave) fall-off of efficiency with frequency has been observed whose origin has not yet been identified. It is speculated that the low field region near the drain contact might cause this steep fall-off. Future devices therefore will be made with reduced gate-drain distance. That might perhaps enhance efficiency in general.



The work accomplished during the fourth period of the contract ending February 29, 1988 includes:

- device fabrication using E-beam direct wafer writing
- influence of gate length and gate structure on performance
- design of tunable stripline circuits
- broadband amplifiers operated between 30 - 37 GHz
- oscillator efficiency versus frequency

Device structure

E-beam lithography has now been introduced for direct wafer writing. It is now possible to change the device structure quickly.

Two basically different structures have been fabricated: finger gate devices and overlapping gate devices both having 0.5 µm long and 400 µm wide Schottky gates. Since finger gate-devices of the type shown in Fig. 1 are always yielding ten times lower efficiencies (0.1 %) apparently due to the large gate sheet resistance work on this type of device will not be continued.

The second type of device having an overlapping gate with bonding pads on both sides as shown in Fig. 2 is exhibiting efficiency around 1 %. The advantage of this structure is the large gate area yielding extremely low sheet resistance so that large gate widths can be used.

The reduction of gate length from 1.5 µm to 0.5 µm did not result in the expected increase of efficiency which contrary to our believe (see conclusions of the 3rd interim report) indicates that the DC-power dissipated under the gate is not much higher in longer gate devices than in short gate devices. From this we conclude that the optimum gate length is around 1.5 µm which is easy to fabricate.

As will be discussed later another critical device dimension might be the low field region near the drain contact which could be the cause of the observed 12 db/octave fall-off of efficiency.

Circuit configuration

The microstrip circuit configuration used in the present investigation is shown in Fig. 3. The drain contact of the device is connected to the end of a 50 Ω microstrip line. Both gate and source contacts are connected to ($\lambda/2 + \delta$)-transmission lines which are terminated by radial stubs acting as short

circuits. The value of δ determines the magnitude of capacitive reactance necessary for compensating for bonding wire inductances.

a) Small signal impedance

Using a Wiltron 360 Network Analyzer (borrowed from Wiltron Munich) the device impedance has been measured at different lengths L_G and L_S. L_G was varied continuously by using a sliding short ("butterfly"), L_S was fixed and made equal to $\lambda/2$ at 34 GHz. Fig. 4 shows two measured gain versus frequency characteristics. It can be clearly seen that the frequency of maximum gain had been shifted from 29.6 GHz to 33.4 GHz and this was achieved by reducing L_G by 0.4 mm corresponding to 4 GHz. Shifting the gain peak to higher frequencies was not possible with this circuit due to the poor quality of the sliding short above 34 GHz. However, a narrow gain peak was produced at 37 GHz with fixed lengths L_G and L_S corresponding to $\lambda/2$ at 35 GHz. In this case gain was also exhibited between 28 GHz and 33 GHz.

Also shown in Fig. 4 are the measured impedance values at several frequencies. It is interesting to note that negative resistance of the order of -10 Ω to -30 Ω generally appears in series with an inductive reactance. That maximum gain is accompanied by a positive value of reactance (j10 to j100) rather than by zero indicates that other elements such as device capacitance, stripline "gap" capacitance, etc. also play a role in this circuit.

The gain vs. frequency characteristic depends, of course, on both drain and gate bias voltages. Besides the dependence of the magnitude the frequency of maximum gain shifts towards higher frequencies with increasing gate bias voltage indicating that the gate depletion layer capacitance is part of the total device impedance.

b) Oscillator results

FECTEDs mounted in the same microstrip circuits have been made oscillating by placing a dielectric resonator near the drain and gate bonding pads and by slightly increasing bias levels. The frequency of operation has been adjusted by both the lengths L_G and L_S of the $(\lambda/2 + \delta)$-lines and by using a proper dielectric resonator. No simple relation exists between $(\lambda/2 + \delta)$ and the resonance frequency of the dielectric resonator. It was, however, consistently observed that the oscillator frequency is always higher by approximately 1 GHz than the nominal resonator frequency.

Fig. 5 shows a plot of efficiency vs. frequency for a number of devices. The observed fall-off of 12 db per octave is far too steep since the intrinsic device is not transit-time limited and, hence, only an RC-type fall-off

of $1/f^{\alpha}$ with $1 < \alpha < 2$ should occur. In a few cases the efficiency was indeed found to be constant (0.5 %) when the device was tuned from 30 GHz to 35 GHz, but 0.5 % efficiency was low to start with. Whether the generally observed 12 db/octave fall-off is caused by the large gate-drain "gap" capacitance, by the low field region near the drain (series resistance) in conjunction with the high field domain capacitance or by other losses is not yet clear. A reduction of the length of the low field region near the drain might resolve this question. The device impedance must certainly be characterized more thoroughly before final conclusions can be drawn.

Conclusions and Future Research Plan

The work performed during the fourth period of the contract was aimed for identifying the circuit elements responsible for tuning both maximum gain frequency and oscillator frequency. It has been demonstrated that maximum small signal gain occurs near that frequency at which the total reactance is slightly positiv. This was achieved by connecting both source and gate contacts to ground via capacitive impedances provided by shorted ($\lambda/2 + \delta$) lines. The value δ was somewhere between 0 and $\lambda/4$. Oscillations have been obtained with identical circuits by placing a dielectric resonator with a resonance frequency close to the maximum gain frequency near both drain and gate bonding pads. The observed 12 db/octave fall-off of efficiency cannot be explained at present. Circuit parasitics or/and the low field region near the drain contact of the device are made responsible for this steep fall-off. Future work will concentrate on reducing these losses. Also, InP FECTEDs will be made in addition to GaAs devices as InP promises higher efficiency due to the higher peak to valley ratio of the velocity-field characteristic. The goal is to reach the theoretically predicted efficiency levels of the order of 5 % - 10 % in the 35 GHz range.

Personnel

Dr. Kurt Lübke, Helmut Scheiber, Christian Diskus, Gerald Hofmann, Gabriele Roitmayr and Johann Katzenmayer.

Annex

The amount of unused funds remaining on the contract at the end of the period covered by the report is $ 59,000.00 minus $ 14,950.00 for which an invoice has been submitted together with this (fourth) report.

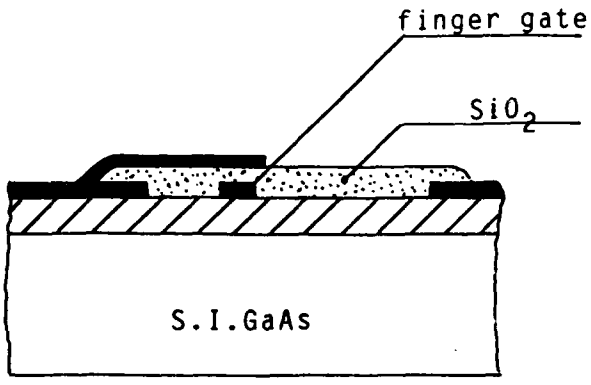


Fig. 1

Cross sectional view of a FECTED with finger gate

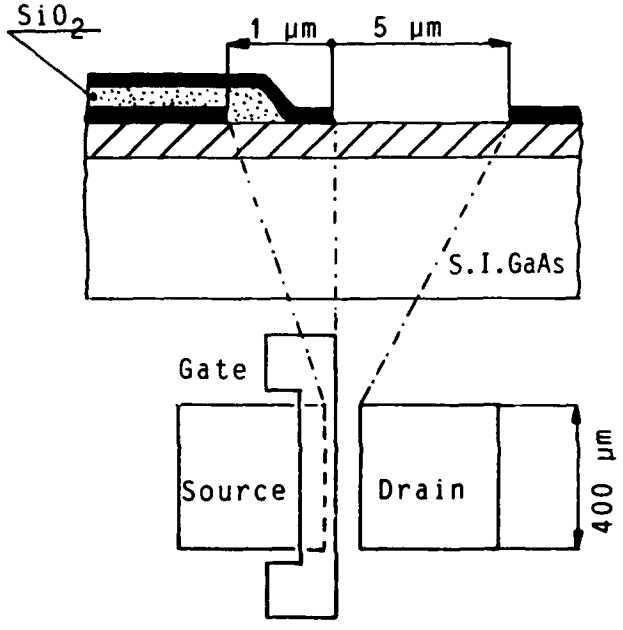


Fig. 2

Cross sectional view and top view of the new overlapping gate FECTED with 0.5 µm gate length

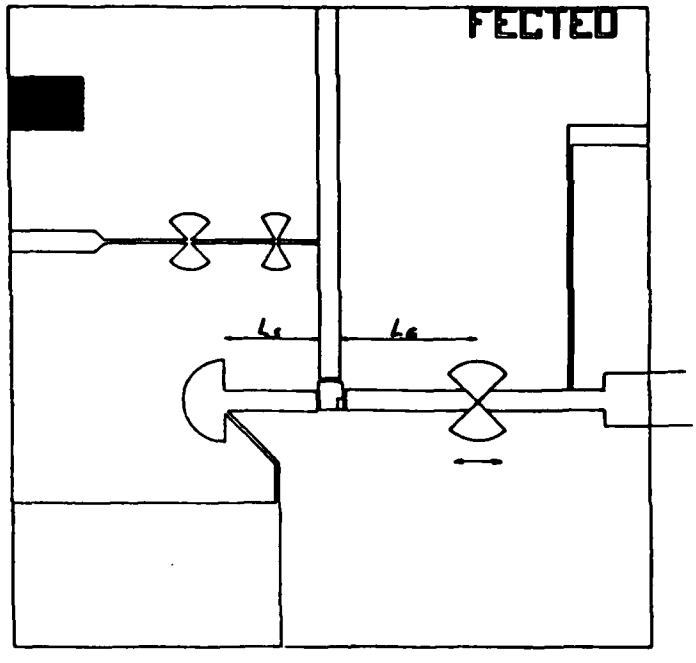


Fig. 3

Microstrip circuit configuration with tunable gate resonator

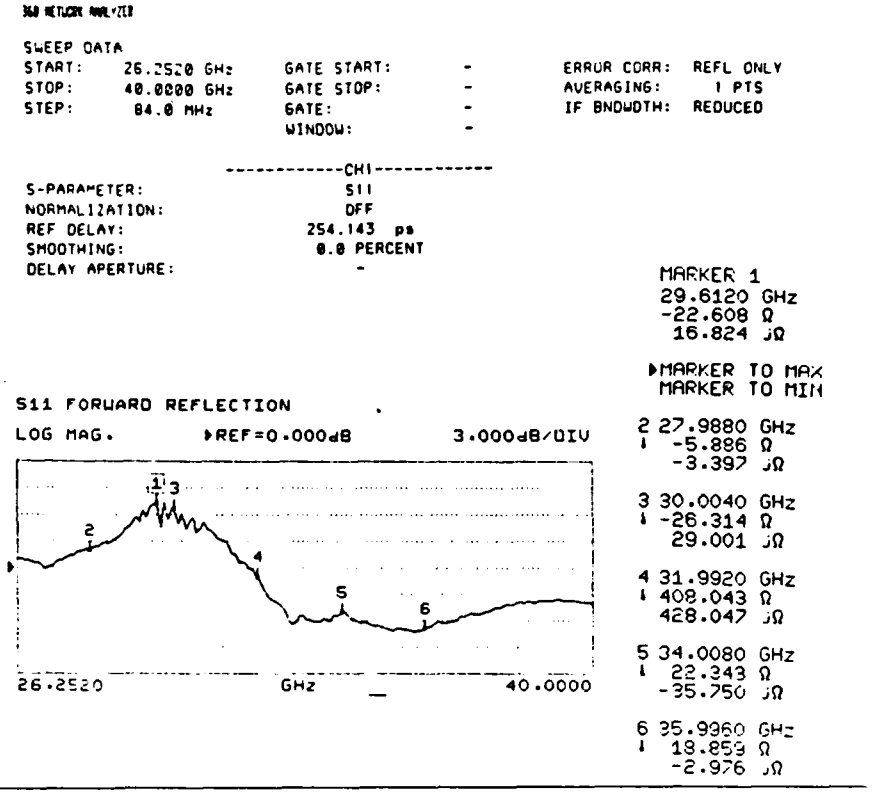


Fig. 4

Gain vs. frequency obtained with FECTED small signal amplifiers

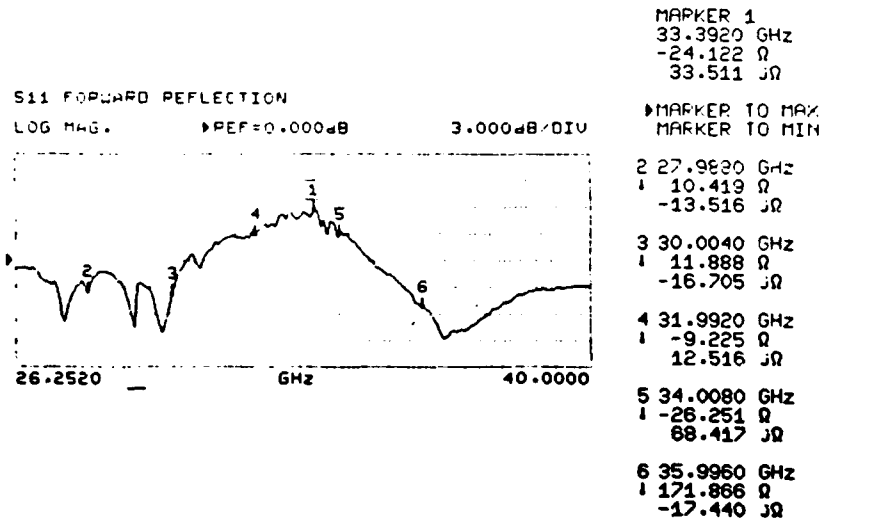
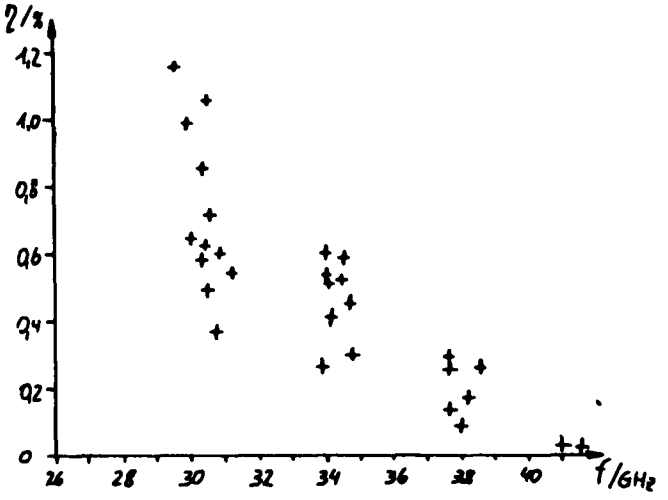
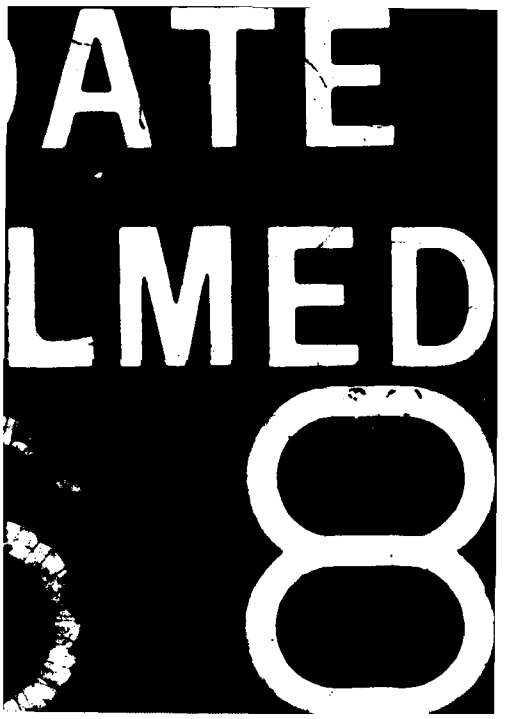


Fig. 5

Efficiencies vs. frequency obtained with FECTED oscillators

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